

Swift Burst Alert Telescope (BAT) Image Processor (IP) / Block Command and Data Handler(BCDH) Interface Test Procedure Rev -

December 10, 2001

Prepared by: B. Settles/561

National Aeronautics and Space Administration Goddard Space Flight Center Greenbelt, Maryland

Prepared By: **Beverly Settles** BAT IP Product Design Lead Code 561 Flight Electronics Branch Reviewed By: BAT IP MIC Design Lead Code 561 Flight Electronics Branch 11/28/01 Reviewed By: Miles Smith Date BAT BCDH Design Lead Code 564 Microelectronics and Signal Processing Branch Reviewed By:

Michelle Scott
BAT IP Test Engineer

Flight Electronics Branch

Code 561

Reviewed By:	Teresa LaFourcade BAT IP Test Engineer Code 561 Flight Electronics Branch	11/6/01 Date
Reviewed By:	Quang Hguyen Group Leader Code 561 Flight Electronics Branch	1 1/07/0) Date
Reviewed By: AL	Michael Kelly Michael Kelly Municipe Municipe Municipe Manage Code303	11 7/6/ Date

System Assurance Management

REVISION PAGE

REVISION	DATE	BY	DESCRIPTION	APPROVED
_	12/10/01	Swift CM Office	Initial Release	Swift CM Office

Introduction

The Image Processor and the Block Command and Data Handler are subsystems on the Swift Burst Alert Telescope. The Image Processor (IP) is a data system required to collect, process, and analyze data that will be transmitted from the BAT instrument front end electronics. The BCDH interfaces to the BAT detector modules to receive Gamma Ray Burst event data.

Purpose

The purpose of this document is to outline the procedure that documents the process required to verify the SpaceWire interface between the Image Processor and the Block Command and Data Handler prior to the release of the ASIC code for both subsystems.

Document Scope

This document outlines the procedure for verification of the IP-BCDH SpaceWire interface. Verification of data shall be performed by the Test Engineers and the BCDH lead engineer per the Swift Burst Alert Telescope Block Command & Data Handler Software Interface Control Document(410.4ICD-0002a).

1.3 Required Hardware

The following components are required for this interface test.

- A. Flight Rad6000 Processor card
- B. ETU Bulk Memory/1553 card
- C. Breadboard MIC card
- D. Demo2 or ETU BCDH
- E. BCDH Simulator(if available)
- F. BVR Simulator
- G. Power Supplies
- H. 15-ft MIC-to-BCDH interface cable
- I. MIC Loopback cables

Applicable Documents

Standards

GPG-8730.1 Calibration and Metrology

NASA-STD-8739.7 Electrostatic Discharge Control

Procedures

410.4-PROC-0064 Swift Burst Alert Telescope MIC GSE and BCDH ETU to IP Multi- Channel

Interface Card Safe-to-Mate

2.3 Documents

410.4-ICD-0002a Swift Burst Alert Telescope Block Command & Data Handler Software Interface

Control Document

BAT DM Controller Specification Draft 5 7-31-01

Block Command and Data Handler Hardware Interface Control Document, Rev F, $7/16/01\,$

Swift Burst Alert Telescope (BAT) Image Processor (IP)Interface Control Document

410.4-PLAN-0006 Burst Alert Telescope Parts Control Plan

410-4-PG-8730.3.3 Swift Quality Management Plan

410-SPEC-002 Swift Mission Assurance Requirements Document,

Quality Provisions

Stated below are the Quality Provisions for Quality Assurance (QA) as they relate to this interface test.

Test shall be in accordance with the Swift Mission Assurance Requirements Document, GSFC-SWIFT-410-SPEC-002 and the Swift Quality Management Plan, 410-4-PG-8730.3.3 and the 410.4-PLAN-0006 Burst Alert Telescope Parts Control Plan.

Test Conduct

The performance of operations specified in this procedure requires the presence of the Quality Assurance representative, unless waived by the QA representative. QA shall be notified 24 hours prior to the start of the test. QA shall be notified at test completion to review data recorded in this procedure. As applicable, the Test Engineer shall certify the GSE required for the test is complete by verifying that it is in calibration. Upon completion of the test, the resultant test data shall be attached to this test procedure.

3.2 Failure Criteria

The inability of the device under test (BCDH or IP) to perform its required functions, as specified, during test operation shall be considered a failure.

3.3 Failure Reports

Malfunction or failure reporting shall be in accordance with the Swift Quality Management Plan. All anomalies resulting from this test shall be documented in the Image Processor log book. Problems relating to the SpaceWire interface shall be documented on the Problem Record form.

3.4 Test Conditions

- a. Temperature: 18.3 degrees C to 27.8 degrees C (65 degrees F to 82 degrees F)
- b. Relative Humidity 30% to 70%
- c. ESD Protection: Equal to Requirements defined in GSFC ESD NASA-STD-8739.7.

3.5 Procedural Changes

Deviations from this procedure during test shall be red lined on the as run procedure by the cognizant Test Engineer , the PDL or the QA representative.

4 Requirements

4.1 General Requirements

The following general requirements shall be followed during the conduct of this procedure.

4.1.1 Precautions/Operating Instructions

- a) The requirements of proper handling of ESD sensitive hardware shall be followed. Personnel handling the boards shall be ESD certified.
- b) Breast pockets shall be emptied and badges tucked in, prior to working over the circuit cards.

4.1.2 Test Records

All data taken during this test shall be recorded in this procedure. Print outs shall be attached to this procedure. Testing using any flight cards shall be recorded on the WOA for that component; this test procedure shall also be referenced on the WOA.

4.2 Test Equipment

Test equipment used for this test shall be recorded in Table 4.3-1

TABLE 4.3-1 TEST EQUIPMENT LIST			
NOMENCLATURE	MANUFACTURER	NEMS(NASA ID)	Cal. Due Date

4.3.2 Perform a continuity check on any Breakout box(BOB) used during this procedure.

	Test Sequence Initialization
•	Perform the Swift Burst Alert Telescope MIC GSE and BCDH ETU to IP Multi- Channel Interface Card Safe-to-Mate procedure.
	Power up the BCDH e: For BCDH Demo 2 board and the BCDH ETU board, the digital outputs of the 5V, 3.3 and 2.5V supplies must enabled simultaneously.
•	Record the BCDH current:
Rec	ord BCDH 3.3V current Expected(.017A +/005) ord BCDH 2.5V current Expected(.15A +/005) ord BCDH 5.0V current Expected(.05A +/005)
	Power down the BCDH Connect the BCDH to the MIC via the interface cable: Link 14 must be connected to the BCDH ETU board or BCDH Demo 2 board. Connect the loop back cables(J1 and J3) if less than 8 BCDHs are used during this test. Power up the Image Processor Record Image Processor current: 3.3V Current Expected (.924A +/05) Expected (1.769A +/05)
	Power up the BCDH te: For BCDH Demo 2 board and the BCDH ETU board, the digital outputs of the 5V, 3.3 and 2.5V supplies must enabled simultaneously.
•	Record the BCDH current:
Rec	ord BCDH 3.3V current Expected(.017A +/005) ord BCDH 2.5V current Expected(.15A +/005) ord BCDH 5.0V current Expected(.05A +/005)

If 16 links BCDH simulator is used, power and configure the simulator to send the following bit patterns to links to be simulated. Indicate the number of simulated links.:

Note: Data must not be sent to any link connected to a Demo 2 or a BCDH ETU.

Link 1: AAAABBBB Link2: BCDEBCDE Link3: 5A5A5A5A Link4: BABEBABE Link5: FACEFACE Link 6: DADEDADE Link 7: ACEDACED Link8: 1A2B3C4D

Link 9: 0000DDDD Link 10: CDEF0000 Link 11 5A6A7A8A Link 12 BBB9AAA9 Link 13 EDCBEDCB Link 14 ECAFECAF Link 15 DECADECA Link 16 9B239B23

5.2	Configuration: 1 ETU BCDH or Demo 2 Board and 2 MIC Loopback Cables(J1 and J3) Execute script <i>Startup.scr</i> to configure the Image Processor and to verify the aliveness of the Image Processor MIC, Bulk Memory and the BCDH.
No	te: The <i>Startup.scr</i> script will perform the following functions:
	Configure the MIC PCI
	Configure the BM PCI
	Reset MIC
	Configure Links to be tested
	Set MIC Max Packet length Set MIC DMA Configuration
	Set MIC DMA Configuration Set MIC DMA Time Out Configuration
•	Power dwn the BCDH
•	Power up the BCDH
•	For Link 14, verify the following is received:
•	For BCDH Demo 2 board:
	1 BCDH Command Verify
	1 BCDH CMD Verify Exception
	4 BCDH DM Command Verify Exceptions
	Verify that the "Cleared Receiver FIFO" bit is set in the BCDH Command Verify
	Exception Packet.
	For BCDH ETU board:
	1 BCDH Command Verify.
	1 BCDH CMD Verify Exception
	16 BCDH DM Command Verify Exceptions:(0x
	Verify that the "Cleared Receiver FIFO" bit is set in the BCDH Command Verify Exception Packet.
	• Execute script <i>BatIP.scr</i> to send the following data patterns to the following links.
	Link 0: AAAABBBB
	Link1: BCDEBCDE
	Link2: 5A5A5A5A
	Link8: BABEBABE
	Link9: FACEFACE
	Link 10: ACEDACED Note: These data patterns are not sent to Link 14.
	Note. These data patterns are not sent to Link 14.
	 Read Bulk Memory(Type d0x88000000,100,4) Verify the simulated link patterns.
3 .7 / /	
Note: S Perforn	See page 11 for expected bit patterns ned byDate
5 3 Co	mmand Verification
	ecute script test 1.scr
2	
The sc	ript test 1.scr will execute the following commands:
	and: BCDH Reset
	and: BCDH Test ADC Mux(1)
Delay(1	sec)
Comma	and: BCDH Test ADC Mux(2)

Continue command-delay sequence through BCDH Test ADC Mux(15) for Demo 2; ADC MUX(7) for ETU.

•	For Link 14, verify the	· · · · · · · · · · · · · · · · · · ·
		For BCDH Demo 2 board:
		1 Reset Command Verify
		1 BCDH Command Verify Exception
		4 BCDH DM Command Verify Exceptions
		16 Test ADC Command Verifys
		Verify that the "Cleared Receiver FIFO" bit is set in the BCDH Command Veri
		Exception Packet.
		LED illumination at 1 sec intervals in increasing 0000h-1111h
		For BCDH ETU board: 1
		1 Reset Command Verify.
		1 BCDH CMD Verify Exception
		16 BCDH DM Command Verify Exceptions:
		7 Test ADC Command Verifys
		Verify that the "Cleared Receiver FIFO" bit is set in the BCDH CMD Verify
		Exception Packet.
No	ote : See page 11 for expe	cted bit patterns

BCDH Data Packet Definitions

Performed by _____Date____

BCDH Data Packet:: BCDH Command Verify	Expected Bit Pattern
Command : BCDH Reset	31-13 Zero
	12-8 Zero
	7 Zero
	6-0 1001011
	(0x0000004b)
BCDH Data Packet:: BCDH DM Command	Expected Bit Pattern
Verify Exception	
	31-18 Zero
	17 1
	16 0
	15-11 11111
	10-8: Demo 2: 000 or 100
	ETU: 000 thru 111
	7: 0 or 1
	6-0 1101011
	(0x0002f86b-)
	(0x0002fc6b)

	(0x0002fceb)
	(0x0002f8eb)
BCDH Data Packet:: BCDH Command Verify	Expected Bit Pattern
Command: BCDH Test ADC Mux	31-13 Zero
	12-8 10101
	7 Zero
	6-0 1001011
	(0x000154b)

BCDH Data Packet:: BCDH Command Verify	Expected Bit Pattern
Exception	1
	31-19 Zero
	18 1
	17-13 0
	12-8 00000 ETU
	12-8 10101 Demo 2
	7 Zero
	6-0 1001011ETU
	6-0 1101101 Demo2
	(0x000154b) Demo 2
	(0x0004006d) ETU

5.4 Non-Continuos Data Verification

• Execute script *Test2.scr*

The script *test2.scr* will execute the following commands

Command: BCDH Request Status Command: BCDH Request Version Command: BCDH Echo Absolute Time Stamp

• Verify the following data packets from Link 14:

A. Status Data Verification

BCDH Status Data Packet

Request Status Command Verify Packet

Note: Record SpaceWire Status bit in table below.

BCDH Data Packet: BCDH Status	Expected Bit Pattern
DW0	31-16 Zero
	15 1
	14-11 Zero
	10 1
	9-7 000
	6-0 1001101b
	(0X0000844D)
DW1	31-11 Zero
	10 1
	9-7 Zero
	6 0 or 1
	5-4 Zero
	3-0 0001

	(0X00000441)
DW2	31-26 Demo2: 0 ETU : 1 25-24 1 23-18 Demo2: 0 ETU : 1 17-16 1 15-4 Zero 3-0 0001 (0X03030001) DEMO 2 (0XFFFF0001) ETU
DW3	31-16 Space Wire Status Register A Bits 15-4 Zero 3-0 0001 (0XE0440001) DEMO 2 (0XE9440001) ETU
DW4	31-16 Space Wire Status Register B Bits 15-9 Zero Demo 2 15-9 00000010 ETU 8 1 7-4 Zero 3-0 0001 (0X50000001 OR 0X1000001) DEMO 2 (0X10000201) ETU

BCDH Data Packet:: BCDH	Expected Bit Pattern
Command Verify	
Command: BCDH Request Status	31-13 Zero
_	12-8 01000
	7 Zero
	6-0 1001011
	(01/00000017)
	(0X0000084B)

410.4-PROC-0	055
Revision (-)	

Performed by	Date

BCDH Request Version Packet Request Version Command Verify Packet Note: Due to changes in the versions, these bits a Record the bit pattern in the table below. Verify data with BCDH lead engineer.	are not static and are subject to change
BCDH Data Packet: BCDH Version	Expected Bit Pattern
	31-24 Zero 23-16 Demo 2: 00001000 ETU: 11100001 15-8 Demo 2: 00010000 ETU: 00000101 7 Zero 6-0 1011111 (0X00080C5F) DEMO 2 (0X00E1055F) ETU
BCDH Data Packet:: BCDH Command Verify	Expected Bit Pattern
Command: BCDH Request Version	31-13 ZERO 12-8 10011 7-4 0100 3-0 1011 (0X0000134B) CHANGES

Performed by _____Date____

Note: Value of BCDH packet	will depend on	contents of data in script file.

• Record MET set in Script File:	
----------------------------------	--

- Record UTC set in Script File:
- Record UTC correction (bit 19-4 of DW2)

	T 7		~	. •	
•	1/	arı	+1	cati	an

- 1. Record contents of the BCDH Absolute Time Stamp Packet in table below.
- 2. Compare Table contents with Script file contents.
- 3. Absolute Time Stamp Echo Command Verify

BCDH Data Packet: BCDH Absolute Time Stamp Echo	Expected Bit Pattern
DW0	31-8:MSB of MET 7Zero 6-0 1000011 (0X00000043)
DW1	31-24: LSB of MET 23-4: MSB of UTC 3-0 0001 (0x0a000001)
DW2	31-20 LSB of UTC 19-4: 16 bit UTC corr 3-0 0001 (0x00f00051)

BCDH Data Packet:: BCDH Command Verify	Expected Bit Pattern
Command: BCDH Echo Absolute Time	31-13 Zero
Stamp	12-8 00011
	7 0
	6-0 1001011
	(0X0000034B)

 Print Results 		
Performed by	Date	

5.5 Continuous Event Count Data Verification

• Execute script test3.scr

The script *test3.scr* executes the following commands:

BCDH Enable Event Count Delay(TBD) BCDH Disable Event Count

DCDH Disable Event Count			
• Read data from Bulk Memory Card(Type 0x88	8000000,100,4)		
• Verify the following data packets from Link 14	• Verify the following data packets from Link 14:		
a. Command Verify: BCDH Enable Event Countb. Events Count Packetsc. Command Verify: BCDH Disable Event Count			
• Print data			
BCDH Data Packet:: BCDH Command Verify	Expected Bit Pattern		
Command: BCDH Enable Event Count	31-13 Zero 12-8 00110 7 Zero 6-0 1001011 (0X0000064B)		
BCDH Data Packet: BCDH Block Events Count	Expected Bit Pattern		
DWO	(0x0000005)		
DW1 occurs every second	(0x0000001)		
	1=		
BCDH Data Packet:: BCDH Command Verify Command : BCDH Disable Events Count	Expected Bit Pattern 31-14 Zero 12-8 00111 7 Zero 6-0 1001011 (0X0000074B)		
Performed byDate			

5.6 Continuous Time Stamp Data Verification

• Execute script test4.scr

The script *test4.scr* sends the following commands: BCDH Enable TimeStamp Transmit Delay(TBD)
BCDH Disable TimeStamp Transmit

- Read Data from Bulk Memory Card (Type 0x88000000,100,4)
- Verify the following data from Link 14:
- a. Command Verify: BCDH Enable TimeStamp Transmit
- b. BCDH Time Stamp Packet Contents
- c. Command Verify: BCDH Disable TimeStamp Transmit

BCDH Data Packet:: BCDH Command Verify	Expected Bit Pattern
Command: BCDH Enable TimeStamp	31-13 Zero 12-8 00100 7 Zero 6-0 1001011
	(0X000044B)

t Pattern
ng time(0-99)
ıg

BCDH Data Packet:: BCDH Command Verify	Expected Bit Pattern
Command: BCDH Disable TimeStamp	31-13 Zero
	12-8 00101
	7 Zero
	6-0 1001011
	(0X0000054B)

Performed by Date

5.7 Error Injection

a.	Invalid	Commands

• Run script *test5a.scr*

The script *test5a.scr* sends an invalid command (0x0000003F) to the BCDH with the following format:

•	Read Bulk Memory, Type 0x88000000,100,4	
•	Record bit pattern of command sent(3D or 3F).	
•	Verify that a BCDH CMD Verify Exception is received.	
•	Verify that the Invaid CMD bit will be set(bit 16).	

• Print Results.

b. Transmission Interruption

• Run script test5b..scr

The script *test5b.scr* sends the command to start the event count on Link 14.

- Disconnect the interface cable between the IP and BCDH.
- Reconnect the cable.
- Verify the occurrence of the error bits in SpaceWire status register Link 14._____
- Verify successful data transmission has resumed.
- Type *bcdhCmd(0xe,0x4000)*; this stops the event counts.
- Print Results.

c. Parity Error

• Run script test5c.scr

The script test5c.scr sends the command to start event count on Link 14 then sends a parity error on Link 14.

•	Read Bulk Memory, Type 0x88000000,100,4	
•	Verify error marker (0x0000007c) was captured in data stream	·
•	Type $bcdhCmd(0xe,0x4000)$; this stops the event counts.	

Print Results.

Performed by _____ Date

5.8 Interface Characterization

- Insert breakout box between IP and BCDH.
- Execute script signal.scr.
- Using an oscilloscope, capture and print the waveforms of the following signals:
 - a. Data
 - b. Data Strobe
 - c. 1PPS
 - d. 32 MHz Clock
 - e. Command
 - f. Command Strobe

•	Label each waveform and attach to procedure.	
•	Measure frequency of the 32 MHz clock:	
•	Measure frequency and duty cycle of 1 PPS signal	

Performed by	Date

Appendix A. BCDH Command and Packet Formats

Table 1 Commands

Category Command	Cmd Code	Description
------------------	----------	-------------

		msb - Isb	
	BCDH Reset	00000	Resets the BCDH and all of the digital circuits on the board.
Reset	BCDH Reset DM	00001	Resets the DMs specified in the DM Destination Mask.
	BCDH Reset Data FIFO	00010	Resets the Data FIFO and programs the FIFO's programmable half-full flag
	BCDH Echo Absolute Timestamp	00011	An absolute timestamp is embedded in this command, which is then echoed back in the BCDH data stream.
Timestamp	BCDH Enable Timestamp Tx	00100	Enables the autonomous transmission of a 10-msec timestamp packet.
	BCDH Disable Timestamp Tx	00101	Disables the autonomous transmission of a 10-msec timestamp packet.
Event Count	BCDH Enable Event Count Tx	00110	Enables the autonomous transmission of an 8-usec event count packet.
	BCDH Disable Event Count Tx	00111	Disables the autonomous transmission of an 8-usec event count packet.
Status	BCDH Request Status	01000	Request for a BCDH status packet.
DAC Outroute	BCDH Set Common Bias Voltages	01001	Sets eight common bias voltages that are distributed to all DMs within the Block.
DAC Outputs	BCDH Set High Voltage Control Levels	01010	Sets eight control levels that are sent to the BVR to control the eight High Voltages.
High Voltage	BCDH Enable High Voltages	01011	Enables all eight of the High Voltages at once.
Switch	BCDH Disable High Voltages	01100	Disables all eight of the High Voltages at once.

Category	Command	Cmd Code	Description
		msb - Isb	
	BCDH Request Common Bias Voltages	01101	Request for a housekeeping packet containing the current Common Bias Voltage levels
	BCDH Request High Voltage Control Levels	01110	Request for a housekeeping packet containing the current High Voltage control levels (digitized High Voltage DAC outputs).
	BCDH Request DM Power Levels	01111	Request for a housekeeping packet containing the current DM power supply levels
House-keeping	BCDH Request BCDH Power Levels	10000	Request for a housekeeping packet containing the current BCDH power supply levels
	BCDH Request Board Temperatures	10001	Request for a housekeeping packet containing the BCDH, BVR and XA1VR temperatures
	BCDH Request Voltage Ref Levels	10010	Request for a housekeeping packet containing the current voltage reference levels
	BCDH Request High Voltage Monitor Levels	11000	Request for a housekeeping packet containing the current High Voltage monitor levels (digitized voltage that is proportional to the actual High Voltage output from the BVR).
	BCDH Request Version	10011	Request for the current version of the BCDH Verilog firmware.
Debug (only used in Demo2 and the ETU)	BCDH Change Testpoint Mux	10100	Changes which testpoints internal to the Xilinx FPGA are output to the logic analyzer testports A, B and C
	BCDH Test ADC Multiplexers	10101	Changes the four multiplexer select pins, which can be verified through the four LEDs
	BCDH Configure DM	10110	Configures the DM Xilinx FPGA
Loopback	BCDH Loopback	10111	This command is used to loop simulated DM data out of the DM transmitter back to the DM receiver.

Category	Command	Cmd Code	Description
		msb - Isb	
SpaceWire Configuration	BCDH Change SpaceWire Configuration	11001	This command is used to change the SpaceWire configuration on the BCDH side. It can be used to change the data transmit rate, as well as reset the SpaceWire link.
Spares	Spare	11010	Spare command code
	Spare	11011	Spare command code
	Spare	11100	Spare command code
	Spare	11101	Spare command code
	Spare	11110	Spare command code
	Spare	11111	Spare command code

Table 2 Generated Data Packets

Data Packet	Data Code	Description
	msb - Isb	
BCDH Block Event Counts	x x x - 0 1 0 1	Four 2-msec counts of all the normal and raw events within the Block.
Data Continuation Marker	x x x - 0 0 0 1	Indicates that this DWord is a continuation of the previously defined Data Type
BCDH Absolute Timestamp Echo	100-0011	The BCDH receives an absolute timestamp from the IPE every second. This packet echoes the absolute timestamp back to the IPE so it will be included in the data and will provide a time reference.
BCDH Timestamp	100-0111	10-msec timestamp
BCDH Command Verify	100-1011	Verification packet that shows that the BCDH received and acted upon the specified command.
BCDH Status	100-1101	Status

Data Packet	Data Code	Description
	msb - Isb	
BCDH Common Bias Voltages	100-1111	ADC values of the common bias voltages generated by the BCDH
BCDH High Voltage Control Levels	101-0011	ADC values of the high voltage control levels generated by the BCDH
BCDH DM Power Levels	101-0111	ADC values of the DM power levels
BCDH Power Levels	101-1001	ADC values of the BCDH power levels
BCDH Board Temperatures	101-1011	ADC values of the BCDH, the BVR, and the XA1VR board temperatures
BCDH Voltage Ref Levels	101-1101	ADC values of the voltage references generated by the BCDH
BCDH Version	101-1111	Version number of the BCDH (used only in the FPGA version)
BCDH High Voltage Monitor Levels	110-0011	ADC values of the voltages that are proportional to the actual high voltages generated by the BVR.
BCDH DM Parity Error	110-0111	Error packet generated by the BCDH in response to getting a parity error in a DM packet
BCDH DM Command Verify Exception	110-1011	If a DM does not respond to a command by providing a command verify within a specific period of time, or if the command verify is invalid, the BCDH will generate this exception packet
BCDH Spare	110-1101	Spare
BCDH Spare	110-1111	Spare
BCDH Spare	111-0011	Spare
BCDH Spare	111-0111	Spare
BCDH Spare	111-1001	Spare
BCDH Spare	111-1011	Spare